

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 12. (Canceled)

1        13. (Currently Amended) A digital system having a  
2 microprocessor operable to execute a rounding dot product  
3 instruction, wherein the microprocessor comprises:

4        storage circuitry for holding pairs of elements;

5        a multiply circuit connected to receive a first number of  
6 pairs of elements from the storage circuitry in a first execution  
7 phase of the microprocessor responsive to the dot product  
8 instruction, the multiply circuit comprising a plurality of  
9 multipliers equal to the first number of pairs of elements;

10       an adder/subtractor circuit having a plurality of inputs  
11 each connected to receive a corresponding one of the plurality of  
12 products from the plurality of multipliers and a mid-position  
13 carry input to a predetermined bit for mid-position rounding  
14 responsive to the rounding dot product instruction; and

15       a shifter connected to receive an output of the ~~arithmetic~~  
16 adder/subtractor circuit, the shifter operable to shift a  
17 selected amount in response to the rounding dot product  
18 instructions.

Claims 14 to 24. (Canceled)

1        25. (New) A data processing apparatus comprising:

2        a first multiply circuit having first and second inputs and  
3 an output, said first multiply circuit operable in response to a  
4 dot product instruction to multiply data received at said first  
5 and second inputs and generate a first product at said output;

6        a second multiply circuit having first and second inputs and  
7        an output, said second multiply circuit operable in response to a  
8        dot product instruction to multiply data received at said first  
9        and second inputs and generate a second product at said output;  
10       an adder/subtractor circuit having first and second inputs,  
11       a mid-position carry input to a predetermined bit and an output,  
12       said first input receiving said first product from said first  
13       multiply circuit, said second input receiving said second product  
14       from said second multiply circuits, said adder/subtractor circuit  
15       operable in response to said dot product instruction to  
16       arithmetically combine said first and second products and a "1"  
17       input at said mid-position carry input of said predetermined bit  
18       thereby forming a mid-position rounded sum; and  
19       a shifter connected to receive said mid-position rounded sum  
20       of the adder/subtractor circuit, the shifter operable to shift  
21       said mid-position rounded sum a predetermined amount in response  
22       to said dot product instruction.

1       26. (New) The data processing apparatus of claim 25,  
2       wherein:  
3       said arithmetic combination of said first and second  
4       products is an arithmetic sum.

1       27. (New) The data processing apparatus of claim 25,  
2       wherein:  
3       said dot product instruction is a dot product with negate  
4       instruction; and  
5       said arithmetic combination of said first and second  
6       products is a difference of said second product from said first  
7       product in response to said dot product with negate instruction.

1        28. (New) The data processing apparatus of claim 25,  
2 further comprising:

3        a first Q shifter having an input receiving said first  
4 product from said first multiply circuit and an output supplying  
5 said first input to said adder/subtractor circuit, said first Q  
6 shifter shifting said first product an instruction specified  
7 number of bits; and

8        a second Q shifter having an input receiving said second  
9 product from said second multiply circuit and an output supplying  
10 said second input to said adder/subtractor circuit, said second Q  
11 shifter shifting said second product said instruction specified  
12 number of bits.

1        29. (New) The data processing apparatus of claim 25,  
2 wherein:

3        said first multiply generates said first product in a  
4 redundant sign/magnitude format;

5        said second multiply circuit generates said second product  
6 in said redundant sign/magnitude format;

7        said adder/subtractor circuit arithmetically combines said  
8 first and second products and said "1" input at said mid-position  
9 carry input forming said mid-position rounded sum in said  
10 redundant sign/magnitude format;

11       a shifter shifts said mid-position rounded sum in said  
12 redundant sign/magnitude format; and

13       said data processing apparatus further comprises a carry  
14 save adder to 2's complement converter having an input receiving  
15 said shifted mid-position rounded sum in said redundant  
16 sign/magnitude format and an output generating a corresponding  
17 normal coded format.